VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examination 2018 – 19
Outcome Based Education(OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2018 – 19)

VI SEMESTER

Sl. No	Course and Course code		Course Title	Teaching Department	Teaching Hours /Week			Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P					
1	PCC	18EC61	Digital Communication		3	2	--	03	40	60	100	4
2	PCC	18EC62	Embedded Systems		3	2	--	03	40	60	100	4
3	PCC	18EC63	Microwave & Antennas		3	2	--	03	40	60	100	4
4	PEC	18XX64X	Professional Elective -1		3	--	--	03	40	60	100	3
5	OEC	18XX65X	Open Elective –A		3	--	--	03	40	60	100	3
6	PCC	18ECL66	Embedded Systems Laboratory		--	2	2	03	40	60	100	2
7	PCC	18ECL67	Communication Laboratory		--	2	2	03	40	60	100	2
8	MP	18ECMP68	Mini-project		--	--	2	03	40	60	100	2
9	Internship	--	Internship	To be carried out during the vacation/s of VI and VII semesters and /or VII and VIII semesters.								
				TOTAL	**15**	**10**	**6**	**24**	**320**	**480**	**800**	**24**

Note: PCC: Professional core, PEC: Professional Elective, OE: Open Elective, MP: Mini-project.

Professional Elective -1

Course code under 18XX64X	Course Title
18EC641	Operating System
18EC642	Artificial Neural Networks
18EC643	Object Oriented Programming using C++
18EC644	Digital System Design using Verilog
18EC645	Nanoelectronics

Open Elective –A

(i) 18EC651 Signal Processing (ii) 18EC652 Sensors & Signal Conditioning

Students can select any one of the open electives offered by other Departments except those that are offered by the parent Department (Please refer to the list of open electives under 18XX65X).

Selection of an open elective shall not be allowed if,

- The candidate has studied the same course during the previous semesters of the programme.
- The syllabus content of open elective is similar to that of the Departmental core courses or professional electives.
- A similar course, under any category, is prescribed in the higher semesters of the programme.

Registration to electives shall be documented under the guidance of Programme Coordinator/ Advisor/Mentor.

Mini-project work:

Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary Mini- project can be assigned to an individual student or to a group having not more than 4 students.

CIE procedure for Mini-project:

(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.

The CIE marks awarded for the Mini-project work, shall be based on the evaluation of project report, project presentation skill and question and answer session in the ratio 50:25:25.The marks awarded for the project report shall be the same for all the batch mates.

(ii) Interdisciplinary: Continuous Internal Evaluation shall be group wise at the college level with the participation of all the guides of the college.

The CIE marks awarded for the Mini-project, shall be based on the evaluation of project report, project presentation skill and question and answer session in the ratio 50:25:25.The marks awarded for the project report shall be the same for all the batch mates.

SEE for Mini-project:

(i) Single discipline: Contribution to the Mini-project and the performance of each group member shall be assessed individually in the semester end examination (SEE) conducted at the department.

(ii) Interdisciplinary: Contribution to the Mini-project and the performance of each group member shall be assessed individually in semester end examination (SEE) conducted separately at the departments to which the student/s belong to.

Internship: All the students admitted to III year of BE/B.Tech shall have to undergo mandatory internship of 4 weeks during the vacation of VI and VII semesters and /or VII and VIII semesters. A University examination shall be conducted during VIII semester and the prescribed credit shall be included in VIII semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take-up/complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the internship requirements.

AICTE activity Points: In case students fail to earn the prescribed activity Points, Eighth semester Grade Card shall be issued only after earning the required activity Points. Students shall be admitted for the award of degree only after the release of the Eighth semester Grade Card.

BE 2018 Scheme Sixth Semester EC Syllabus

DIGITAL COMMUNICATION **SEMESTER – VI (EC/TC)** **[As per Choice Based Credit System (CBCS) Scheme]**			
Course Code	**18EC61**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03 + 02 (Tutorial)**	**SEE Marks**	**60**
		Exam Hours	**03**
CREDITS – 04			

Course Objectives: This course will enable students to:

- Understand the mathematical representation of signal, symbol, and noise.
- Understand the concept of signal processing of digital data and signal conversion to symbols at the transmitter and receiver.
- Compute performance metrics and parameters for symbol processing and recovery in ideal and corrupted channel conditions.
- Compute performance parameters and mitigate channel induced impediments in corrupted channel conditions.

Module-1	**RBT Level**
Bandpass Signal to Equivalent Low pass: Hilbert Transform, Pre-envelopes, Complex envelopes, Canonical representation of bandpass signals, Complex low pass representation of bandpass systems, Complex representation of band pass signals and systems **(Text 1: 2.8, 2.9, 2.10, 2.11, 2.12, 2.13).** **Line codes:** Unipolar, Polar, Bipolar (AMI) and Manchester code and their power spectral densities **(Text 1: Ch 6.10).** Overview of HDB3, B3ZS, B6ZS **(Ref. 1: 7.2)**	**L1,L2, L3**
Module-2	
Signaling over AWGN Channels- Introduction, Geometric representation of signals, Gram-Schmidt Orthogonalization procedure, Conversion of the continuous AWGN channel into a vector channel, Optimum receivers using coherent detection: ML Decoding, Correlation receiver, matched filter receiver **(Text 1: 7.1, 7.2, 7.3, 7.4).**	**L1,L2, L3**
Module – 3	
Digital Modulation Techniques: Phase shift Keying techniques using coherent detection: generation, detection and error probabilities of BPSK and QPSK, M–ary PSK, M–ary QAM **(Relevant topics in Text 1 of 7.6, 7.7).** Frequency shift keying techniques using Coherent detection: BFSK generation, detection and error probability **(Relevant topics in Text 1 of 7.8).** Non coherent orthogonal modulation techniques: BFSK, DPSK Symbol representation, Block diagrams treatment of Transmitter and Receiver, Probability of error (without derivation of probability of error equation) **(Text 1: 7.11, 7.12. 7.13).**	**L1,L2, L3**

Module-4	
Communication through Band Limited Channels: Digital Transmission through Band limited channels: Digital PAM Transmission through Band limited Channels, Signal design for Band limited Channels: Design of band limited signals for zero ISI–The Nyquist Criterion (statement only), Design of band limited signals with controlled ISI-Partial Response signals, Probability of error for detection of Digital PAM: Probability of error for detection of Digital PAM with Zero ISI, Symbol–by–Symbol detection of data with controlled ISI **(Text 2: 9.1, 9.2, 9.3.1, 9.3.2).** Channel Equalization: Linear Equalizers (ZFE, MMSE), **(Text 2: 9.4.2).**	**L1,L2, L3**
Module-5	
Principles of Spread Spectrum: Spread Spectrum Communication Systems: Model of a Spread Spectrum Digital Communication System, Direct Sequence Spread Spectrum Systems, Effect of De-spreading on a narrowband Interference, Probability of error (statement only), Some applications of DS Spread Spectrum Signals, Generation of PN Sequences, Frequency Hopped Spread Spectrum, CDMA based on IS-95 **(Text 2: 11.3.1, 11.3.2, 11.3.3, 11.3.4, 11.3.5, 11.4.2).**	**L1,L2, L3**
Course Outcomes: At the end of the course, the students will be able to: • Associate and apply the concepts of Band pass sampling to well specified signals and channels. • Analyze and compute performance parameters and transfer rates for low pass and band pass symbol under ideal and corrupted non band limited channels. • Test and validate symbol processing and performance parameters at the receiver under ideal and corrupted band limited channels. • Demonstrate that band pass signals subjected to corruption and distortion in a band limited channel can be processed at the receiver to meet specified performance criteria.	
Question paper pattern: • Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks. • Each full question can have a maximum of 4 sub questions. • There will be 2 full questions from each module covering all the topics of the module. • Students will have to answer 5 full questions, selecting one full question from each module. • The total marks will be proportionally reduced to 60 marks as SEE marks is 60.	
Text Books: 1. Simon Haykin, "Digital Communication Systems", John Wiley & sons, First Edition, 2014, ISBN 978-0-471-64735-5. 2. John G Proakis and Masoud Salehi, "Fundamentals of Communication Systems", 2014 Edition, Pearson Education, ISBN 978-8-131-70573-5.	

Reference Books:

1. B.P.Lathi and Zhi Ding, “Modern Digital and Analog communication Systems”, Oxford University Press, 4th Edition, 2010, ISBN: 978-0-198-07380-2.
2. Ian A Glover and Peter M Grant, “Digital Communications”, Pearson Education, Third Edition, 2010, ISBN 978-0-273-71830-7.
3. Bernard Sklar and Ray, "Digital Communications - Fundamentals and Applications", Pearson Education, Third Edition, 2014, ISBN: 978-81-317-2092-9.

EMBEDDED SYSTEMS

SEMESTER – VI (EC/TC)

[As per Choice Based Credit System (CBCS) Scheme]

Course Code	**18EC62**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03+2 (Tutorial)**	**SEE Marks**	**60**
		Exam Hours	**03**

CREDITS – 04

Course objectives: This course will enable students to:

- Explain the architectural features and instructions of 32 bit microcontroller - ARM Cortex M3.
- Develop Programs using the various instructions of ARM Cortex M3 and C language for different applications.
- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Develop the hardware software co-design and firmware design approaches.
- Explain the need of real time operating system for embedded system applications.

Module 1	**RBT Level**
ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, Debugging support, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence **(Text 1: Ch-1, 2, 3)**	**L1,L2**
Module 2	
ARM Cortex M3 Instruction Sets and Programming: Assembly basics, Instruction list and description, Thumb and ARM instructions, Special instructions, Useful instructions, CMSIS, Assembly and C language Programming **(Text 1: Ch-4, Ch-10.1 to 10.6)**	**L1,L2, L3**
Module 3	
Embedded System Components: Embedded Vs General computing system, Classification of Embedded systems, Major applications and purpose of ES. Elements of an Embedded System (Block diagram and explanation), Differences between RISC and CISC, Harvard and Princeton, Big and Little Endian formats, Memory (ROM and RAM types), Sensors, Actuators, Optocoupler, Communication Interfaces (I2C, SPI, IrDA, Bluetooth, Wi-Fi, Zigbee only) **(Text 2: All the Topics from Ch-1 and Ch-2 (Fig and explanation before 2.1) 2.1.1.6 to 2.1.1.8, 2.2 to 2.2.2.3, 2.3 to 2.3.2, 2.3.3.3, selected topics of 2.4.1 and 2.4.2 only)**.	**L1,L2**

Module 4	
Embedded System Design Concepts: Characteristics and Quality Attributes of Embedded Systems, Operational and non-operational quality attributes, Embedded Systems-Application and Domain specific, Hardware Software Co-Design and Program Modeling (excluding UML), Embedded firmware design and development (excluding C language). **Text 2: Ch-3, Ch-4 (4.1, 4.2.1 and 4.2.2 only), Ch-7 (Sections 7.1, 7.2 only), Ch-9 (Sections 9.1, 9.2, 9.3.1, 9.3.2 only)**	**L1,L2, L3**
Module 5	
RTOS and IDE for Embedded System Design: Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock, Concept of Binary and counting semaphores (Mutex example without any program), How to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil), Disassembler/decompiler, simulator, emulator and debugging techniques **(Text 2: Ch-10 (Sections 10.1, 10.2, 10.3, 10.5.2 , 10.7, 10.8.1.1, 10.8.1.2, 10.8.2.2, 10.10 only), Ch-12, Ch-13 (a block diagram before 13.1, 13.3, 13.4, 13.5, 13.6 only)**	**L1,L2, L3**

Course outcomes: After studying this course, students will be able to:

- Describe the architectural features and instructions of 32 bit microcontroller ARM Cortex M3.
- Apply the knowledge gained for Programming ARM Cortex M3 for different applications.
- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Develop the hardware software co-design and firmware design approaches.
- Explain the need of real time operating system for embedded system applications.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M3”, 2nd Edition, Newnes, (Elsevier), 2010.

2. Shibu K V, “Introduction to Embedded Systems”, Tata McGraw Hill Education Private Limited, 2nd Edition.

Reference Books:

1. James K. Peckol, "Embedded systems- A contemporary design tool", John Wiley, 2008, ISBN: 978-0-471-72180-2.

2. Yifeng Zhu, “Embedded Systems with Arm Cortex-M Microcontrollers in Assembly Language and C”, 2nd E -Man Press LLC ©2015 ISBN:0982692633 9780982692639.

3. Embedded real time systems by K.V. K. K Prasad, Dreamtech publications, 2003.

4. Embedded Systems by Rajkamal, 2nd Edition, McGraw hill Publications, 2010.

MICROWAVE and ANTENNAS SEMESTER – VI EC [As per Choice Based Credit System (CBCS)			
Course Code	**18EC63**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03+02 (Tutorial)**	**SEE Marks**	**60**
		Exam Hours	**03**
CREDITS – 04			

Course objectives: This course will enable students to:

- Describe the microwave properties and its transmission media
- Describe microwave devices for several applications
- Understand the basics of antenna theory
- Select antennas for specific applications

Module 1	**RBT Level**
Microwave Tubes: Introduction, Reflex Klystron Oscillator, Mechanism of Oscillations, Modes of Oscillations, Mode Curve (Qualitative Analysis only). **(Text 1: 9.1, 9.2.1)** **Microwave Transmission Lines:** Microwave Frequencies, Microwave devices, Microwave Systems, Transmission Line equations and solutions, Reflection Coefficient and Transmission Coefficient, Standing Wave and Standing Wave Ratio, Smith Chart, Single Stub matching. **(Text 2: 0.1, 0.2, 0.3, 3.1, 3.2, 3.3, 3.5, 3.6 Except Double stub matching**)	**L1,L2**
Module 2	
Microwave Network theory: Introduction**,** Symmetrical Z and Y-Parameters for reciprocal Networks, S matrix representation of Multi-Port Networks. **(Text1: 6.1, 6.2, 6.3)** **Microwave Passive Devices:** Coaxial Connectors and Adapters, Attenuators, Phase Shifters, Waveguide Tees, Magic tees. **(Text 1: 6.4.2, 6.4.14, 6.4.15, 6.4.16)**	**L1,L2**
Module 3	
Strip Lines: Introduction, Micro Strip lines, Parallel Strip lines, Coplanar Strip lines, Shielded Strip Lines**. (Text 2: 11.1, 11.2, 11.3, 11.4)** **Antenna Basics**: Introduction, Basic Antenna Parameters, Patterns, Beam Area, Radiation Intensity, Beam Efficiency, Directivity and Gain, Antenna Apertures, Effective Height, Radio Communication Link, Antenna Field Zones. **(Text 3: 2.1 - 2.7, 2.9 – 2.11, 2.13)**	**L1,L2,L3**
Module 4	

Point Sources and Arrays: Introduction, Point Sources, Power Patterns, Power Theorem, Radiation Intensity, Arrays of two isotropic point sources, Linear Arrays of n Isotropic Point Sources of equal Amplitude and Spacing. **(Text 3: 5.1 – 5.6, 5.9, 5.13)** **Electric Dipoles:** Introduction, Short Electric Dipole, Fields of a Short Dipole, Radiation Resistance of a Short Electric Dipole, Thin Linear Antenna (Field Analyses) **(Text 3: 6.1 - 6.5)**	**L1,L2,L3,L4**
Module 5	
Loop and Horn Antenna: Introduction, Small loop, The Loop Antenna General Case, The Loop Antenna as a special case, Radiation resistance of loops, Directivity of Circular Loop Antennas with uniform current, Horn antennas Rectangular Horn Antennas. **(Text 3: 7.1, 7.2, 7.4, 7.6, 7.7, 7.8, 7.19, 7.20)** **Antenna Types**: The Helix geometry, Helix modes, Practical Design considerations for the mono-filar axial mode Helical Antenna, Yagi-Uda array, Parabolic reflector **(Text 3: 8.3, 8.4, 8.5, 8.8, 9.5)**	**L1,L2,L3**

Course outcomes: At the end of the course students will be able to:

- Describe the use and advantages of microwave transmission
- Analyze various parameters related to microwave transmission lines and waveguides
- Identify microwave devices for several applications
- Analyze various antenna parameters necessary for building a RF system
- Recommend various antenna configurations according to the applications.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. **Microwave Engineering** – Annapurna Das, Sisir K Das, TMH, Publication, 2nd, 2010.
2. **Microwave Devices and circuits**- Samuel Y Liao, Pearson Education
3. **Antennas and Wave Propagation**- John D. Krauss, Ronald J Marhefka, Ahmad S Khan, 4th Edition, McGraw Hill Education, 2013

Reference Books:

1. **Microwave Engineering** - David M Pozar, John Wiley India Pvt. Ltd., 3rd Edn, 2008.
2. **Microwave Engineering** – Sushrut Das, Oxford Higher Education, 2ndEdn, 2015
3. **Antennas and Wave Propagation** – Harish and Sachidananda: Oxford

OPERATING SYSTEM

SEMESTER – VI (EC/TC)

[As per Choice Based Credit System (CBCS) System (CBCS) Scheme]

Course Code	**18EC641**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (8 Hours /Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Objectives: This course will enable students to:

- Understand the services provided by an operating system.
- Explain how processes are synchronized and scheduled.
- Understand different approaches of memory management and virtual memory management.
- Describe the structure and organization of the file system
- Understand interprocess communication and deadlock situations.

Module-1	**RBT Level**
Introduction to Operating Systems OS, Goals of an OS, Operation of an OS, Computational Structures, Resource allocation techniques, Efficiency, System Performance and User Convenience, Classes operating System, Batch processing, Multi programming, Time Sharing Systems, Real Time and distributed Operating Systems **(Topics from Sections 1.2, 1.3, 2.2 to 2.8 of Text).**	**L1,L2**
Module-2	
Process Management: OS View of Processes, PCB, Fundamental State Transitions of a process, Threads, Kernel and User level Threads, Non-preemptive scheduling- FCFS and SRN, Preemptive Scheduling- RR and LCN, Scheduling in Unix and Scheduling in Linux **(Topics from Sections 3.3, 3.3.1 to 3.3.4, 3.4, 3.4.1, 3.4.2 , Selected scheduling topics from 4.2 and 4.3 , 4.6, 4.7 of Text).**	**L1,L2, L3**
Module – 3	
Memory Management: Contiguous Memory allocation, Non-Contiguos Memory Allocation, Paging, Segmentation, Segmentation with paging, Virtual Memory Management, Demand Paging, VM handler, FIFO, LRU page replacement policies, Virtual memory in Unix and Linux **(Topics from Sections 5.5 to 5.9, 6.1 to 6.3 except Optimal policy and 6.3.1, 6.7,6.8 of Text).**	**L1,L2, L3**
Module-4	
File Systems: File systems and IOCS, File Operations, File Organizations, Directory structures, File Protection, Interface between File system and IOCS, Allocation of disk space, Implementing file access	**L1,L2**

(Topics from Sections 7.1 to 7.8 of Text).	
Module-5	
Message Passing and Deadlocks: Overview of Message Passing, Implementing message passing, Mailboxes, Deadlocks, Deadlocks in resource allocation, Handling deadlocks, Deadlock detection algorithm, Deadlock Prevention **(Topics from Sections 10.1 to 10.3, 11.1 to 11.5 of Text).**	**L1,L2**

Course Outcomes: At the end of the course, the students will be able to:

- Explain the goals, structure, operation and types of operating systems.
- Apply scheduling techniques to find performance factors.
- Explain organization of file systems and IOCS.
- Apply suitable techniques for contiguous and non-contiguous memory allocation.
- Describe message passing, deadlock detection and prevention methods.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Operating Systems – A concept based approach, by Dhamdhere, TMH, 2nd edition.

Reference Books:

1. Operating systems concepts, Silberschatz and Galvin, John Wiley India Pvt. Ltd, 5th edition,2001.
2. Operating system–internals and design system, William Stalling, Pearson Education, 4th ed, 2006.
3. Design of operating systems, Tannanbhaum, TMH, 2001.

ARITIFICAL NEURAL NETWORKS

SEMESTER – VI (EC/TC)

[As per Choice Based Credit System (CBCS) System (CBCS) Scheme]

Course Code	**18EC642**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (8 Hours / Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Objectives: This course will enable students to:

- Understand the basics of ANN and comparison with Human brain.
- Acquire knowledge on Generalization and function approximation of various ANN architectures.
- Understand reinforcement learning using neural networks
- Acquire knowledge of unsupervised learning using neural networks.

Module-1	**RBT Leve**
Introduction: Biological Neuron – Artificial Neural Model - Types of activation functions – **Architecture**: Feedforward and Feedback, Convex Sets, Convex Hull and Linear Separability, Non-Linear Separable Problem. XOR Problem, Multilayer Networks. **Learning:** Learning Algorithms, Error correction and Gradient Descent Rules, Learning objective of TLNs, Perceptron Learning Algorithm, Perceptron Convergence Theorem.	**L1, L2**
Module-2	
Supervised Learning: Perceptron learning and Non Separable sets, α-Least Mean Square Learning, MSE Error surface, Steepest Descent Search, μ-LMS approximate to gradient descent, Application of LMS to Noise Cancelling, Multi-layered Network Architecture, Back propagation Learning Algorithm, Practical consideration of BP algorithm.	**L1,L2, L3**
Module-3	
Support Vector Machines and Radial Basis Function: Learning from Examples, Statistical Learning Theory, Support Vector Machines, SVM application to Image Classification, Radial Basis Function Regularization theory, Generalized RBF Networks, Learning in RBFNs, RBF application to face recognition.	**L1,L2, L3**
Module-4	

Attractor Neural Networks: Associative Learning Attractor Associative Memory, Linear Associative memory, Hopfield Network, application of Hopfield Network, Brain State in a Box neural Network, Simulated Annealing, Boltzmann Machine, Bidirectional Associative Memory.	**L1,L2, L3**
Module-5	
Self-organization Feature Map: Maximal Eigenvector Filtering, Extracting Principal Components, Generalized Learning Laws, Vector Quantization, Self-organization Feature Maps, Application of SOM, Growing Neural Gas.	**L1,L2, L3**

Course outcomes: At the end of the course, students should be able to:

- Understand the role of neural networks in engineering, artificial intelligence, and cognitive modelling.
- Understand the concepts and techniques of neural networks through the study of the most important neural network models.
- Evaluate whether neural networks are appropriate to a particular application.
- Apply neural networks to particular application, and to know what steps to take to improve performance.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Neural Networks A Classroom Approach– Satish Kumar, McGraw Hill Education (India) Pvt. Ltd, Second Edition.

Reference Books:

1. **Introduction to Artificial Neural Systems-**J.M. Zurada, Jaico Publications 1994.
2. **Artificial Neural Networks-**B. Yegnanarayana, PHI, New Delhi 1998.

OBJECT ORIENTED PROGRAMMING USING C++

SEMESTER – VI (EC/TC)

[As per Choice Based Credit System (CBCS) System (CBCS) Scheme]

Course Code	**18EC643**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (8 Hours / Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Objectives: The objectives of this course are:

- Define Encapsulation, Inheritance and Polymorphism.
- Solve the problem with object oriented approach.
- Analyze the problem statement and build object oriented system model.
- Describe the characters and behavior of the objects that comprise a system.
- Explain function overloading, operator overloading and virtual functions.
- Discuss the advantages of object oriented programming over procedure oriented programming.

Module-1	**RBT Level**
Beginning with C++ and its features: What is C++?, Applications and structure of C++ program, Different Data types, Variables, Different Operators, expressions, operator overloading and control structures in C++ **(Topics from Ch-2, 3 of Text).**	**L1, L2**
Module-2	
Functions, classes and Objects: Functions, Inline function, function overloading, friend and virtual functions, Specifying a class, C++ program with a class, arrays within a class, memory allocation to objects, array of objects, members, pointers to members and member functions **(Selected Topics from Chap-4, 5 of Text).**	**L1,L2, L3**
Module-3	
Constructors, Destructors and Operator overloading: Constructors, Multiple constructors in a class, Copy constructor, Dynamic constructor, Destructors, Defining operator overloading, Overloading Unary and binary operators, Manipulation of strings using operators **(Selected topics from Chap-6, 7 of Text)**.	**L1, L2, L3**
Module-4	
Inheritance, Pointers, Virtual Functions, Polymorphism: Derived Classes, Single, multilevel, multiple inheritance, Pointers to objects and derived classes, this pointer, Virtual and pure virtual functions **(Selected topics from Chap-8, 9 of Text)**.	**L1, L2, L3**
Module-5	

Streams and Working with files: C++ streams and stream classes, formatted and unformatted I/O operations, Output with manipulators, Classes for file stream operations, opening and closing a file, EOF **(Selected topics from Chap-10, 11 of Text).**	**L1, L2, L3**

Course outcomes: At the end of the course, students should be able to:

- Explain the basics of Object Oriented Programming concepts.
- Apply the object initialization and destroy concept using constructors and destructors.
- Apply the concept of polymorphism to implement compile time polymorphism in programs by using overloading methods and operators.
- Use the concept of inheritance to reduce the length of code and evaluate the usefulness.
- Apply the concept of run time polymorphism by using virtual functions, overriding functions and abstract class in programs.
- Use I/O operations and file streams in programs.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Object Oriented Programming with C++, E. Balaguruswamy, TMH, 6th Edition, 2013.

Reference Books:

1. Object Oriented Programming using C++, Robert Lafore, Galgotia publication 2010.

DIGITAL SYSTEM DESIGN USING VERILOG

SEMESTER – VI EC
[As per Choice Based Credit System (CBCS) System (CBCS) Scheme]

Course Code	**18EC644**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hrs per module)**	**Exam Hours**	**03**

CREDITS – 03

Course Objectives: This course will enable students to

- Understand the concepts of Verilog Language.
- Design the digital systems as an activity in a larger systems design context.
- Study the design and operation of semiconductor memories frequently used in application specific digital system.
- Inspect how effectively IC's are embedded in package and assembled in PCB's for different application.
- Design and diagnosis of processors and I/O controllers used in embedded systems.

Module -1	**RBT Level**
Introduction and Methodology: Digital Systems and Embedded Systems, Real-World Circuits, Models, Design Methodology **(1.1, 1.3 to 1.5 of Text).** **Combinational Basics:** Combinational Components and Circuits, Verification of Combinational Circuits **(2.3 and 2.4 of Text**). **Number Basics:** Unsigned integers, Signed Integers, Fixed point Numbers, Floating point Numbers **(3.1.1, 3.2.1, 3.3.1 and 3.4).** **Sequential Basics**: Sequential Datapaths and Control Clocked Synchronous Timing Methodology **(4.3 up to 4.3.1, 4.4 up to 4.4.1 of Text).**	**L1,L2, L3**
Module -2	
Memories: Concepts, Memory Types, Error Detection and Correction **(Chap 5 of Text).**	**L1,L2, L3**
Module -3	
Implementation Fabrics: Integrated Circuits, Programmable Logic Devices, Packaging and Circuit boards, Interconnection and Signal integrity **(Chap 6 of Text).**	**L1,L2, L3**
Module -4	
I/O interfacing: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software **(Chap 8 of Text).**	**L1,L2, L3**
Module -5	

Design Methodology: Design flow, Design optimization, Design for test, Nontechnical Issues **(Chap 10 of Text).**	**L1,L2, L3, L4**

Course outcomes: After studying this course, students will be able to:

- Construct the combinational circuits, using discrete gates and programmable logic devices.
- Describe how arithmetic operations can be performed for each kind of code, and also combinational circuits that implement arithmetic operations.
- Design a semiconductor memory for specific chip design.
- Design embedded systems using small microcontrollers, larger CPUs/DSPs, or hard or soft processor cores.
- Synthesize different types of I/O controllers that are used in embedded system.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Peter J. Ashenden, "Digital Design: An Embedded Systems Approach Using VERILOG", Elesvier, 2010.

Reference Books:

1. Ming-Bo Lin, "Digital System Designs and Practices: Using Verilog HDL and FPGAs", Wiley, 2008
2. Charles Roth, Lizy K. John, "Byeong Kil LeeDigital Systems Design Using Verilog, Cengage", Cengage, 1st Edition.
3. Donald E. Thomas, Philip R. Moorby, "The Verilog Hardware Description Language", Springer, Fifth edition.
4. Michael D. Ciletti, "Advanced Digital Design with the Verilog HDL" Pearson (Prentice Hall), Second edition.

NANOELECTRONICS

SEMESTER – VI EC

[As per Choice Based Credit System (CBCS) System (CBCS) Scheme]

Course Code	**18EC645**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (8 Hours / Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Objectives: This course will enable students to:

- Enhance basic engineering science and technical knowledge of Nanoelectronics.
- Explain basics of top-down and bottom-up fabrication process, devices and systems.
- Describe technologies involved in modern day electronic devices.
- Know various nanostructures of carbon and the nature of the carbon bond itself.
- Learn the photo physical properties of sensor used in generating a signal.

Module-1	**RBT Level**
Introduction: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moore's law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometer length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems **(Text 1).**	**L1, L2**
Module-2	
Characterization: Classification, Microscopic techniques, Field ion microscopy,scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques **(Text 1).** **Inorganic semiconductor nanostructures:** overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states **(Text 1).**	**L1, L2**
Module-3	
Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, collidal quantum dots, self-assembly techniques. **(Text 1).**	**L1, L2**

Physical processes: modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intraband absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural **(Text 1).**	
Module-4	
Carbon Nanostructures: Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes. **(Text 2)**	**L1, L2**
Module-5	
Nanosensors: Introduction, What is Sensor and Nanosensors?, What makes them Possible?, Order From Chaos, Characterization, Perception, Nanosensors Based On Quantum Size Effects, Electrochemical Sensors, Sensors Based On Physical Properties, Nanobiosensors, Smart dust Sensor for the future. **(Text 3)** **Applications:** Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIP's, NEMS, MEMS **(Text 1).**	**L1, L2**

Course Outcomes: After studying this course, students will be able to:

- Understand the principles behind Nanoscience engineering and Nanoelectronics.
- Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials.
- Know the properties of carbon and carbon nanotubes and its applications.
- Know the properties used for sensing and the use of smart dust sensors.
- Apply the knowledge to prepare and characterize nanomaterials.
- Analyse the process flow required to fabricate state-of-the-art transistor technology.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, "Nanoscale Science and Technology", John Wiley, 2007.
2. Charles P Poole, Jr, Frank J Owens, "Introduction to Nanotechnology", John Wiley, Copyright 2006, Reprint 2011.
3. T Pradeep, "Nano: The essentials-Understanding Nanoscience and Nanotechnology", TMH.

Reference Book:

1. Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, “Hand Book of Nanoscience Engineering and Technology”, CRC press, 2003.

EMBEDDED SYSTEMS LAB
SEMESTER – VI (EC/TC)
[As per Choice Based Credit System (CBCS) System (CBCS) Scheme]

Course Code	**18ECL66**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**02 Hr Tutorial (Instructions) + 02 Hours Laboratory**	**SEE Marks**	**60**
RBT Levels	**L1, L2, L3**	**Exam Hours**	**03**

CREDITS – 02

Course objectives: This course will enable students to:

- Understand the instruction set of ARM Cortex M3, a 32 bit microcontroller and the software tool required for programming in Assembly and C language.
- Program ARM Cortex M3 using the various instructions in assembly level language for different applications.
- Interface external devices and I/O with ARM Cortex M3.
- Develop C language programs and library functions for embedded system applications.

Laboratory Experiments

Conduct the following experiments on an ARM CORTEX M3 evaluation board to learn ALP and using evaluation version of Embedded 'C' & Keil uVision-4 tool/compiler.

PART A:

1. ALP to multiply two 16 bit binary numbers.
2. ALP to find the sum of first 10 integer numbers.
3. ALP to find the number of 0's and 1's in a 32 bit data
4. ALP to find determine whether the given 16 bit is even or odd
5. ALP to write data to RAM

PART B:

6. Display "Hello world" message using internal UART
7. Interface and Control the speed of a DC Motor.
8. Interface a Stepper motor and rotate it in clockwise and anti-clockwise direction.
9. Interface a DAC and generate Triangular and Square waveforms.
10. Interface a 4x4 keyboard and display the key code on an LCD.
11. Demonstrate the use of an external interrupt to toggle an LED On/Off.
12. Display the Hex digits 0 to F on a 7-segment LED interface, with an appropriate delay.

Course outcomes: After studying this course, students will be able to:

- Understand the instruction set of 32 bit microcontroller ARM Cortex M3, and the software tool required for programming in Assembly and C language.
- Develop assembly language programs using ARM Cortex M3 for different applications.
- Interface external devices and I/O with ARM Cortex M3.
- Develop C language programs and library functions for embedded system applications.

Conduction of Practical Examination:

- One Question from PART A and one Question from PART B to be asked in the examination.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

COMMUNICATION LAB
SEMESTER – VI EC
[As per Choice Based Credit System (CBCS) System (CBCS) Scheme]

Course Code	**18ECL67**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**02 Hr Tutorial (Instructions) + 02 Hours Laboratory**	**SEE Marks**	**60**
RBT Levels	**L1, L2, L3**	**Exam Hours**	**03**

CREDITS – 02

Course objectives: This course will enable students to:

- Design and test the communication circuits for different analog modulation schemes.
- Design and demonstrate the digital modulation techniques
- Demonstrate and measure the wave propagation in microstrip antennas
- Characteristics of microstrip devices and measurement of its parameters.
- Understand the probability of error computations of coherent digital modulation schemes.

Laboratory Experiments

PART-A: Experiments No. 1 to 5 has to be performed using discrete components.

1. Amplitude Modulation and Demodulation: i) Standard AM, ii)DSBSC (LM741 and LF398 ICs can be used)
2. Frequency modulation and demodulation (IC 8038/2206 can be used)
3. Pulse sampling, flat top sampling and reconstruction
4. Time Division Multiplexing and Demultiplexing of two bandlimited signals.
5. FSK and PSK generation and detection
6. Measurement of frequency, guide wavelength, power, VSWR and attenuation in microwave test bench.
7. Obtain the Radiation Pattern and Measurement of directivity and gain of microstrip dipole and Yagi antennas.
8. Determination of
    a. Coupling and isolation characteristics of microstrip directional coupler.
    b. Resonance characteristics of microstrip ring resonator and computation of dielectric constant of the substrate.
    c. Power division and isolation of microstrip power divider.

PART-B: Simulation Experiments using SCILAB/MATLAB/Simulink or LabVIEW

1. Simulate NRZ, RZ, half-sinusoid and raised cosine pulses and generate eye diagram for binary polar signaling.
2. Pulse code modulation and demodulation system.
3. Computations of the Probability of bit error for coherent binary ASK, FSK and

PSK for an AWGN Channel and Compare them with their Performance curves.

4. Digital Modulation Schemes i) DPSK Transmitter and receiver, ii) QPSK Transmitter and Receiver.

Course Outcomes: On the completion of this laboratory course, the students will be able to:

- Determine the characteristics and response of microwave waveguide.
- Determine the characteristics of microstrip antennas and devices and compute the parameters associated with it.
- Design and test the digital and analog modulation circuits and display the waveforms.
- Simulate the digital modulation systems and compare the error performance of basic digital modulation schemes.

Conduct of Practical Examination:

- All laboratory experiments are to be considered for practical examination.
- For examination one question from **PART-A** and one question from **PART-B or** only one question from **PART-B** experiments based on the complexity, to be set.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

OPEN ELECTIVES-A OFFERED BY EC/TC BOARD

SIGNAL PROCESSING **SEMESTER – VI** **[As per Choice Based Credit System (CBCS) System (CBCS) Scheme]**			
Course Code	**18EC651**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (8Hours/Module)**	**Exam Hours**	**03**
CREDITS – 03			

Course objective: This course will enable students to:

- Understand, represent and classify continuous time and discrete time signals and systems, together with the representation of LTI systems.
- Ability to represent continuous time signals (both periodic and non-periodic) in the time domain, s-domain and the frequency domain
- Understand the properties of analog filters, and have the ability to design Butterworth filters
- Understand and apply sampling theorem and convert a signal from continuous time to discrete time or from discrete time to continuous time (without loss of information)
- Able to represent the discrete time signal in the frequency domain
- Able to design FIR and IIR filters to meet given specifications

Module-1	**RBT Level**
Signal Definition, Signal Classification, System definition, System classification, for both continuous time and discrete time. Definition of LTI systems **(Chapter 1)**	**L1, L2**
Module-2	
Introduction to Fourier Transform, Fourier Series, Relating the Laplace Transform to Fourier Transform, Frequency response of continuous time systems, **(Chapter 3)**	**L1, L2**
Module-3	
Frequency response of ideal analog filters, Salient features of Butterworth filters Design and implementation of Analog Butterworth filters to meet given specifications **(Chapter 8)**	**L1,L2, L3**
Module-4	
Sampling Theorem- Statement and proof, converting the analog signal to a digital signal. Practical sampling. The Discrete Fourier Transform, Properties of DFT. Comparing the frequency response of analog and digital systems. (FFT not included) **(Chapter 3, 4)**	**L1,L2, L3**
Module-5	
Definition of FIR and IIR filters. Frequency response of ideal digital filters Transforming the Analog Butterworth filter to the Digital IIR Filter using suitable mapping techniques, to meet given specifications. Design of FIR Filters using the Window technique, and the frequency sampling	**L1,L2, L3**

technique to meet given specifications Comparing the designed filter with the desired filter frequency response **(Chapter 8)**	

Course Outcomes: After studying this course, students will be able to:

- Understand and explain continuous time and discrete time signals and systems, in time and frequency domain
- Apply the concepts of signals and systems to obtain the desired parameter/ representation
- Analyse the given system and classify the system/arrive at a suitable conclusion
- Design analog/digital filters to meet given specifications
- Design and implement the analog filter using components/ suitable simulation tools *(assignment component)*
- Design and implement the digital filter (FIR/IIR) using suitable simulation tools, and record the input and output of the filter for the given audio signal *(assignment component)*

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

'Signals and Systems', by Simon Haykin and Barry Van Veen, Wiley.

References:

1. 'Theory and Application of Digital Signal Processing', Rabiner and Gold
2. 'Signals and Systems', Schaum's Outline series
3. 'Digital Signal Processing', Schaum's Outline series

SENSORS and SIGNAL CONDITIONING

SEMESTER – VI Open Elective A

[As per Choice Based Credit System (CBCS) System (CBCS) Scheme]

Course Code	**18EC652**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE marks**	**60**
Total Number of Lecture Hours	**40 (08 Hrs/module)**	**Exam Hours**	**03**

CREDITS – 03

Course Objectives: This course will enable students to:

- Understand various technologies associated in manufacturing of sensors
- Acquire knowledge about types of sensors used in modern digital systems
- Get acquainted about material properties required to make sensors

Module 1	**RBT Level**
Introduction to sensor bases measurement systems: General concepts and terminology, sensor classification, primary sensors, material for sensors, microsensor technology, magnetoresistors, light dependent resistors, resistive hygrometers, resistive gas sensors, liquid conductivity sensors **(Selected topics from ch.1 & 2 of Text)**	**L1, L2**
Module 2	
Reactance Variation and Electromagnetic Sensors: -Capacitive Sensors, Inductive Sensors, Electromagnetic Sensors. **Signal Conditioning for Reactance Variation Sensors**-Problems and Alternatives, ac Bridges Carrier Amplifiers, Coherent Detection, Specific Signal Conditioners for Capacitive Sensors, Resolver-to-Digital and Digital-to-Resolver Converters.	**L1, L2**
Module 3	
Self-generating Sensors-Thermoelectric sensors, piezoelectric sensors, pyroelectric sensors, photovoltaic sensors, electrochemical sensors.	**L2,L3**
Module 4	
Digital and intelligent sensors-position encoders, resonant sensors, sensors based on quartz resonators, SAW sensors, Vibrating wire strain gages, vibrating cylinder sensors, Digital flow meters.	**L2,L3**
Module 5	
Sensors based on semiconductor junctions - Thermometers based on semiconductor junctions, magneto diodes and magneto transistors, photodiodes and phototransistors, sensors based on MOSFET transistors, charge- coupled sensors – types of CCD imaging sensors, ultrasonic-based sensors.	**L2,L3**

Course Outcomes: After studying this course, students will be able to:

- Appreciate various types of sensors and their construction
- Use sensors specific to the end use application
- Design systems integrated with sensors

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

"Sensors and Signal Conditioning", Ramon Pallás Areny, John G. Webster, 2nd edition, John Wiley and Sons, 2000