VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examination 2018 – 19
Outcome Based Education(OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2018 – 19)

VII SEMESTER

Sl. No	Course and Course code		Course Title	Teaching Department	Teaching Hours /Week			Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P					
1	PCC	18EC71	Computer Networks		3	--	--	03	40	60	100	3
2	PCC	18EC72	VLSI Design		3	--	--	03	40	60	100	3
3	PEC	18XX73X	Professional Elective - 2		3	--	--	03	40	60	100	3
4	PEC	18XX74X	Professional Elective - 3		3	--	--	03	40	60	100	3
5	OEC	18XX75X	Open Elective -B		3	--	--	03	40	60	100	3
6	PCC	18ECL76	Computer Networks Lab		--	2	2	03	40	60	100	2
7	PCC	18ECL77	VLSI Laboratory		--	2	2	03	40	60	100	2
8	Project	18ECP78	Project Work Phase - 1		--	--	2	--	100	--	100	1
9	Internship	--	Internship	(If not completed during the vacation of VI and VII semesters, it shall be carried out during the vacation of VII and VIII semesters)								
				TOTAL	**15**	4	**6**	**21**	**380**	**420**	**800**	**20**

Note: PCC: Professional core, PEC: Professional Elective.

Professional Elective - 2

Course code under 18XX73X	Course Title
18EC731	Real Time System
18EC732	Satellite Communication
18EC733	Digital Image Processing
18EC734	Data Structures using C++
18EC735	DSP Algorithms & Architecture

Professional Electives - 3

Course code under 18XX74X	Course Title
18EC741	IOT & Wireless Sensor Networks
18EC742	Automotive Electronics
18EC743	Multimedia Communication
18EC744	Cryptography
18EC745	Machine Learning

Open Elective –B

(i) 18EC751 Communication Theory (ii) 18EC752 Neural Networks

Students can select any one of the open electives offered by other Departments except those that are offered by the parent Department (Please refer to the list of open electives under 18XX75X).

Selection of an open elective shall not be allowed if,

- The candidate has studied the same course during the previous semesters of the programme.
- The syllabus content of open elective is similar to that of the Departmental core courses or professional electives.
- A similar course, under any category, is prescribed in the higher semesters of the programme.

Registration to electives shall be documented under the guidance of Programme Coordinator/ Advisor/Mentor.

Project work:

Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary project can be assigned to an individual student or to a group having not more than 4 students. In extraordinary cases, like the funded projects requiring students from different disciplines, the project student strength can be 5 or 6.

CIE procedure for Project Work Phase - 1:

(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.

The CIE marks awarded for the project work phase -1, shall be based on the evaluation of the project work phase -1 Report (covering Literature Survey, Problem identification, Objectives and Methodology), project presentation skill and question and answer session in the ratio 50:25:25.The marks awarded for the Project report shall be the same for all the batch mates.

(ii) Interdisciplinary: Continuous Internal Evaluation shall be group wise at the college level with the participation of all guides of the college. Participation of external guide/s, if any, is desirable.

The CIE marks awarded for the project work phase -1, shall be based on the evaluation of project work phase -1 Report, project presentation skill and question and answer session in the ratio 50:25:25.The marks awarded for the project report shall be the same for all the batch mates.

Internship: All the students admitted to III year of BE/B.Tech shall have to undergo mandatory internship of 4 weeks during the vacation of VI and VII semesters and /or VII and VIII semesters. A University examination shall be conducted during VIII semester and the prescribed credit shall be included in VIII semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take-up/complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the internship requirements.

AICTE activity Points: In case students fail to earn the prescribed activity Points, Eighth semester Grade Card shall be issued only after earning the required activity Points. Students shall be admitted for the award of degree only after the release of the Eighth semester Grade Card.

BE 2018 Scheme Seventh Semester EC Syllabus

COMPUTER NETWORKS

B.E., VII Semester, Electronics & Communication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Course Code	18EC71	CIE Marks	40
Number of Lecture Hours/Week	3	SEE Marks	60
Total Number of Lecture Hours	40 (08 Hours / Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course will enable students to:

- Understand the layering architecture of OSI reference model and TCP/IP protocol suite.
- Understand the protocols associated with each layer.
- Learn the different networking architectures and their representations.
- Learn the functions and services associated with each layer.

Module-1	RBT Level
Introduction: Data communication: Components, Data representation, Data flow, Networks: Network criteria, Physical Structures, Network types: LAN, WAN, Switching, The Internet. **(1.1, 1.2, 1.3(1.3.1 to 1.3.4 of Text).** **Network Models:** Protocol Layering: Scenarios, Principles, Logical Connections, TCP/IP Protocol Suite: Layered Architecture, Layers in TCP/IP suite, Description of layers, Encapsulation and Decapsulation, Addressing, Multiplexing and Demultiplexing, The OSI Model: OSI Versus TCP/IP. **(2.1, 2.2, 2.3 of Text)**	**L1, L2**
Module-2	
Data-Link Layer: Introduction: Nodes and Links, Services, Two Categories' of link, Sublayers, Link Layer addressing: Types of addresses, ARP. Data Link Control (DLC) services: Framing, Flow and Error Control, Data Link Layer Protocols: Simple Protocol, Stop and Wait protocol, Piggybacking. **(9.1, 9.2 (9.2.1, 9.2.2), 11.1, 11.2 of Text)** **Media Access Control:** Random Access: ALOHA, CSMA, CSMA/CD, CSMA/CA. **(12.1 of Text).** **Wired and Wireless LANs:** Ethernet Protocol, Standard Ethernet. Introduction to wireless LAN: Architectural Comparison, Characteristics, Access Control**. (13.1, 13.2(13.2.1 to 13.2.5), 15.1 of Text)**	**L1,L2, L3**
Module-3	
Network Layer: Introduction, Network Layer services: Packetizing, Routing and Forwarding, Other services, Packet Switching: Datagram Approach, Virtual Circuit Approach, IPV4 Addresses: Address Space, Classful Addressing, Classless Addressing, DHCP, Network Address Resolution, Forwarding of IP Packets: Based on destination Address and Label. **(18.1, 18.2, 18.4, 18.5.1, 18.5.2 of Text)** **Network Layer Protocols:** Internet Protocol (IP): Datagram Format, Fragmentation, Options, Security of IPv4 Datagrams. **(19.1 of Text)**.	**L1,L2, L3**

Unicast Routing: Introduction, Routing Algorithms: Distance Vector Routing, Link State Routing, Path vector routing. **(20.1, 20.2 of Text)**	
Module-4	
Transport Layer: Introduction: Transport Layer Services, Connectionless and Connection oriented Protocols, Transport Layer Protocols: Simple protocol, Stop and wait protocol, Go-Back-N Protocol, Selective repeat protocol. **(23.1, 23.2.1, 23.2.2, 23.2.3, 23.2.4 of Text)** **Transport-Layer Protocols in the Internet:** User Datagram Protocol: User Datagram, UDP Services, UDP Applications, Transmission Control Protocol: TCP Services, TCP Features, Segment, Connection, State Transition diagram, Windows in TCP, Flow control, Error control, TCP congestion control. **(24.2, 24.3.1, 24.3.2, 24.3.3, 24.3.4, 24.3.5, 24.3.6, 24.3.7, 24.3.8, 24.3.9 of Text)**	**L1,L2, L3**
Module-5	
Application Layer: Introduction: providing services, Application- layer paradigms, Standard Client –Server Protocols: World wide web, Hyper Text Transfer Protocol, FTP: Two connections, Control Connection, Data Connection, Electronic Mail: Architecture, Wed Based Mail, Telnet: Local versus remote logging. Domain Name system: Name space, DNS in internet, Resolution, DNS Messages, Registrars, DDNS, security of DNS. **(25.1, 26.1, 26.2, 26.3, 26.4, 26.6 of Text)**	**L1, L2**

Course Outcomes: At the end of the course, the students will be able to:

- Understand the concepts of networking thoroughly
- Identify the protocols and services of different layers.
- Distinguish the basic network configurations and standards associated with each network.
- Analyze a simple network and measurement of its parameters.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

TEXT BOOK:

Forouzan, “Data Communications and Networking” , 5th Edition, McGraw Hill, 2013, ISBN: 1-25-906475-3.

REFERENCE BOOKS:

1. James J Kurose, Keith W Ross, Computer Networks, , Pearson Education.
2. Wayarles Tomasi , Introduction to Data Communication and Networking, Pearson Education.
3. Andrew Tanenbaum, “Computer networks”, Prentice Hall.
4. William Stallings, “Data and computer communications”, Prentice Hall,

VLSI DESIGN
SEMESTER – VII EC

[As per Choice Based Credit System (CBCS) scheme]

Course Code	18EC72	CIE Marks	40
Number of Lecture Hours/Week	03	SEE Marks	60
Total Number of Lecture Hours	40 (08 Hours / Module)	Exam Hours	03

CREDITS – 03

Course Objectives: The objectives of the course is to enable students to:

- Impart knowledge of MOS transistor theory and CMOS technologies
- Learn the operation principles and analysis of inverter circuits.
- Design Combinational, sequential and dynamic logic circuits as per the requirements
- Infer the operation of Semiconductors Memory circuits.
- Demonstrate the concepts of CMOS testing

Module-1	RBT Level
Introduction: A Brief History, MOS Transistors, CMOS Logic **(1.1 to 1.4 of TEXT 2)** **MOS Transistor Theory:** Introduction, Long-channel I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics **(2.1, 2.2, 2.4 and 2.5 of TEXT 2).**	**L1, L2**
Module-2	
Fabrication: CMOS Fabrication and Layout, VLSI Design Flow, Introduction, CMOS Technologies, Layout Design Rules, **(1.5 and 3.1 to 3.3 of TEXT 2).** MOSFET Scaling and Small-Geometry Effects, MOSFET Capacitances **(3.5 to 3.6 of TEXT 1)**	**L1, L2,**
Module-3	
Delay: Introduction, Transient Response, RC Delay Model, Linear Delay Model, Logical Efforts of Paths **(4.1 to 4.5 of TEXT 2, except sub-sections 4.3.7, 4.4.5, 4.4.6, 4.5.5 and 4.5.6).** **Combinational Circuit Design:** Introduction, Circuit families **(9.1 to 9.2 of TEXT 2, except subsection 9.2.4).**	**L1, L2, L3**
Module-4	
Sequential Circuit Design: Introduction, Circuit Design for Latches and Flip-Flops **(10.1 and 10.3.1 to 10.3.4 of TEXT 2)** **Dynamic Logic Circuits:** Introduction, Basic Principles of Pass Transistor Circuits, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques **(9.1, 9.2, 9.4 to 9.5 of TEXT 1)**	**L1, L2, L3**
Module-5	
Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM), **(10.1 to 10.3 of TEXT 1)** **Testing and Verification:** Introduction, Logic Verification Principles, Manufacturing Test Principles, Design for testability **(15.1, 15.3, 15.5 15.6.1 to 15.6.3 of TEXT 2).**	**L1, L2**

Course outcomes: At the end of the course, the students will be able to:

- Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.
- Draw the basic gates using the stick and layout diagrams with the knowledge of physical design aspects.
- Demonstrate ability to design Combinational, sequential and dynamic logic circuits as per the requirements
- Interpret Memory elements along with timing considerations
- Interpret testing and testability issues in VLSI Design

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

TEXT BOOKS:

1. "CMOS Digital Integrated Circuits: Analysis and Design" - **Sung Mo Kang & Yosuf Leblebici,** Third Edition, Tata McGraw-Hill.

2. "CMOS VLSI Design- A Circuits and Systems Perspective"- Neil H. E. Weste, and David Money Harris 4th Edition, Pearson Education.

REFERENCE BOOKS:

1. Adel Sedra and K. C. Smith, "Microelectronics Circuits Theory and Applications", 6th or 7th Edition, Oxford University Press, International Version, 2009.
2. Douglas A Pucknell & Kamran Eshragian, "Basic VLSI Design", PHI 3rd Edition, (original Edition – 1994).
3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", TMH, 2007.

Professional Elective – 2

REAL TIME SYSTEM
SEMESTER – VII (EC/TC)

[As per Choice Based Credit System (CBCS) scheme]

Course Code	**18EC731**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours per Module)**	**Exam Hours**	**03**

Credits – 03

Course Objectives: This Course will enable students to:

- Understand the fundamentals of Real-time systems and its classifications.
- Describe the concepts of computer control and hardware components for Real-Time Application.
- Discuss the languages to develop software for Real-Time Applications.
- Explain the concepts of operating system and RTS development methodologies.

Module-1	**RBT Levels**
Introduction to Real-Time Systems: Historical background, Elements of a Computer Control System, RTS- Definition, Classification of Real-time Systems, Time Constraints, Classification of Programs. **Concepts of Computer Control:** Introduction, Sequence Control, Loop Control, Supervisory Control, Centralized Computer Control, Hierarchical Systems. **(Text: 1.1 to 1.6 and 2.1 to 2.6)**	**L1, L2**
Module-2	
Computer Hardware Requirements for Real-Time Applications: Introduction, General Purpose Computer, Single Chip Microcomputers and Microcontrollers, Specialized Processors, Process-Related Interfaces, Data Transfer Techniques, Communications, Standard Interface. **(Text: 3.1 to 3.8).**	**L1, L2**
Module-3	
Languages for Real-Time Applications: Introduction, Syntax Layout and Readability, Declaration and Initialization of Variables and Constants, Cutlass, Modularity and Variables, Compilation of Modular Programs, Data types, Control Structures, Exception Handling, Low-level facilities, Co-routines, Interrupts and Device Handling, Concurrency, Real-Time Support, Overview of Real-Time Languages. **(Text: 5.1 to 5.14).**	**L1,L2, L3**
Module-4	
Operating Systems: Introduction, Real-Time Multi-Tasking OS, Scheduling Strategies, Priority Structures, Task Management, Scheduler and Real-Time Clock Interrupt Handler, Memory Management, Code Sharing, Resource Control, Task Co-Operation and Communication, Mutual Exclusion.**(Text: 6.1 to 6.11).**	**L1, L2**
Module-5	
Design of RTS – General Introduction: Introduction, Specification	**L1, L2, L3**

Document, Preliminary Design, Single-Program Approach, Foreground/Background System. **RTS Development Methodologies:** Introduction, Yourdon Methodology, Ward and Mellor Method, Hately and Pirbhai Method. **(Text: 7.1 to 7.5 and 8.1, 8.2, 8.4, 8.5).**	

Course Outcomes: At the end of the course, students should be able to:

- Explain the fundamentals of Real time systems and its classifications.
- Understand the concepts of computer control and the suitable computer hardware requirements for real-time applications.
- Describe the operating system concepts and techniques required for real time systems.
- Develop the software algorithms using suitable languages to meet Real time applications.
- Apply suitable methodologies to design and develop Real-Time Systems.

Text Book:

Real-Time Computer Control, by Stuart Bennet, 2nd Edn. Pearson Education. 2008.

Reference Books:

1. C.M. Krishna, Kang G. Shin, "Real –Time Systems", McGraw –Hill International Editions, 1997.
2. Real-Time Systems Design and Analysis, Phillip. A. Laplante, second edition, PHI, 2005.
3. Embedded Systems, Raj Kamal, Tata McGraw Hill, India, third edition, 2005.

SATELLITE COMMUNICATION

SEMESTER – VII (EC/TC)

[As per Choice Based Credit System (CBCS) scheme]

Course Code	18EC732	CIE Marks	40
Number of Lecture Hours/Week	03	SEE Marks	60
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course will enable students to

- Understand the basic principle of satellite orbits and trajectories.
- Study of electronic systems associated with a satellite and the earth station.
- Understand the various technologies associated with the satellite communication.
- Focus on a communication satellite and the national satellite system.
- Study of satellite applications focusing various domains services such as remote sensing, weather forecasting and navigation.

Module-1	RBT Level
Satellite Orbits and Trajectories: Definition, Basic Principles, Orbital parameters, Injection velocity and satellite trajectory, Types of Satellite orbits, Orbital perturbations, Satellite stabilization, Orbital effects on satellite's performance, Eclipses, Look angles: Azimuth angle, Elevation angle.	**L1, L2**
Module-2	
Satellite subsystem: Power supply subsystem, Attitude and Orbit control, Tracking, Telemetry and command subsystem, Payload. **Earth Station:** Types of earth station, Architecture, Design considerations, Testing, Earth station Hardware, Satellite tracking.	**L1, L2**
Module-3	
Multiple Access Techniques: Introduction, FDMA (No derivation), SCPC Systems, MCPC Systems, TDMA, CDMA, SDMA. **Satellite Link Design Fundamentals**: Transmission Equation, Satellite Link Parameters, Propagation considerations	**L1,L2, L3**
Module-4	
Communication Satellites: Introduction, Related Applications, Frequency Bands, Payloads, Satellite Vs. Terrestrial Networks, Satellite Telephony, Satellite Television, Satellite radio, Regional satellite Systems, National Satellite Systems.	**L1, L2**
Module-5	
Remote Sensing Satellites: Classification of remote sensing systems, orbits, Payloads, Types of images: Image Classification, Interpretation, Applications. **Weather Forecasting Satellites**: Fundamentals, Images, Orbits, Payloads, Applications. **Navigation Satellites**: Development of Satellite Navigation Systems, GPS system, Applications.	**L1,L2, L3**

Course Outcomes: At the end of the course, the students will be able to:

- Describe the satellite orbits and its trajectories with the definitions of parameters associated with it.
- Describe the electronic hardware systems associated with the satellite subsystem and earth station.
- Describe the various applications of satellite with the focus on national satellite system.
- Compute the satellite link parameters under various propagation conditions with the illustration of multiple access techniques.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Anil K. Maini, Varsha Agrawal, Satellite Communications, Wiley India Pvt. Ltd., 2015, ISBN: 978-81-265-2071-8.

Reference Books :

1. Dennis Roddy, Satellite Communications, 4th Edition, McGraw- Hill International edition, 2006
2. Timothy Pratt, Charles Bostian, Jeremy Allnutt, Satellite Communications, 2nd Edition, Wiley India Pvt. Ltd , 2017, ISBN: 978-81-265-0833-4

DIGITAL IMAGE PROCESSING
SEMESTER – VII (EC/TC)

[As per Choice Based Credit System (CBCS) scheme]

Course Code	18EC733	CIE Marks	40
Number of Lecture Hours/Week	03	SEE Marks	60
Total Number of Lecture Hours	40 (08 Hours per Module)	Exam Hours	03
CREDITS – 03			

Course Objectives: This course will enable students to

- Understand the fundamentals of digital image processing.
- Understand the image transforms used in digital image processing.
- Understand the image enhancement techniques used in digital image processing.
- Understand the image restoration techniques and methods used in digital image processing.
- Understand the Morphological Operations used in digital image processing.

Module1	RBT Level
Digital Image Fundamentals: What is Digital Image Processing?, Origins of Digital Image Processing, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Elements of Visual Perception, Image Sensing and Acquisition **(Text: Chapter 1 and Chapter 2: Sections 2.1 to 2.2, 2.6.2)**	**L1,L2**
Module -2	
Image Enhancement in the Spatial Domain: Image Sampling and Quantization, Some Basic Relationships Between Pixels, Linear and Nonlinear Operations. Some Basic Intensity Transformation Functions, Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters **(Text: Chapter 2: Sections 2.3 to 2.62 , Chapter 3: Sections 3.2 to 3.6)**	**L1,L2**
Module -3	
Frequency Domain: Preliminary Concepts, The Discrete Fourier Transform (DFT) of Two Variables, Properties of the 2-D DFT, Filtering in the Frequency Domain, Image Smoothing and Image Sharpening Using Frequency Domain Filters, Selective Filtering. **(Text: Chapter 4: Sections 4.2, 4.5 to 4.10)**	**L1,L2**
Module -4	

Restoration: Noise models, Restoration in the Presence of Noise Only using Spatial Filtering and Frequency Domain Filtering, Linear, Position- Invariant degradations, Estimating the Degradation Function, Inverse Filtering, Minimum Mean Square Error (Wiener) Filtering, Constrained Least Squares Filtering. **(Text: Chapter 5: Sections 5.2, to 5.9)**	**L1,L2**
Module -5	
Morphological Image Processing: Preliminaries, Erosion and Dilation, Opening and Closing. Color Image Processing: Color Fundamentals, Color Models, Pseudocolor Image Processing. **(Text: Chapter 6: Sections 6.1 to 6.3 Chapter 9: Sections 9.1 to 9.3)**	**L1,L2**

Course Outcomes: At the end of the course, students should be able to:

- Understand image formation and the role human visual system plays in perception of gray and color image data.
- Apply image processing techniques in both the spatial and frequency (Fourier) domains.
- Design and evaluate image analysis techniques
- Conduct independent study and analysis of Image Enhancement and restoration techniques.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Digital Image Processing- Rafel C Gonzalez and Richard E. Woods, PHI 3rd Edition 2010.

Reference Books:

1. Digital Image Processing- S.Jayaraman, S.Esakkirajan, T.Veerakumar, Tata McGraw Hill 2014.
2. Fundamentals of Digital Image Processing-A. K. Jain, Pearson 2004.
3. Image Processing analysis and Machine vision with MindTap by Milan Sonka and Roger Boile, Cengage Publications, 2018.

DATA STRUCTURES USING C++
B.E., VII Semester (EC/TC)

[Choice Based Credit System (CBCS) scheme]

Course Code	18EC734	CIE Marks	40
Number of Lecture Hours/Week	3	SEE Marks	60
Total Number of Lecture Hours	40 (8 Hours /Module)	Exam Hours	03

CREDITS – 03

Course objectives: This course will enable students to

- Explain fundamentals of data structures and their applications essential for programming/problem solving
- Analyze Linear Data Structures: Stack, Queues, Lists
- Analyze Non Linear Data Structures: Trees
- Assess appropriate data structure during program development/Problem Solving

Module -1	RBT Level
INTRODUCTION: Functions and parameters, Dynamic memory allocation, Recursion. **LINEAR LISTS:** Data objects and structures, Linear list data structures, Array Representation, Vector Representation, Singly Linked lists and chains.	L1, L2
Module -2	
ARRAYS AND MATRICS: Arrays, Matrices, Special matrices, Sparse matrices. **STACKS:** The abstract data types, Array Representation, Linked Representation, and Applications-Parenthesis Matching & Towers of Hanoi.	L1, L2
Module -3	
QUEUES: The abstract data types, Array Representation, Linked Representation, Applications-Railroad car arrangement. **HASHING:** Dictionaries, Linear representation, Hash table representation.	L1, L2, L3
Module -4	
BINARY AND OTHER TREES: Trees, Binary trees, Properties and representation of binary trees, Common binary tree operations, Binary tree traversal the ADT binary tree, ADT binary tree and the class linked binary tree.	L1,L2 ,L3
Module -5	
Priority Queues: Linear lists, Heaps, Applications-Heap Sorting. **Search Trees:** Binary search trees operations and implementation, Binary Search trees with duplicates.	L1, L2,L3

Course outcomes: After studying this course, students will be able to:

- Acquire knowledge of Dynamic memory allocation, Various types of data structures, operations and algorithms and Sparse matrices and Hashing
- Understand non Linear data structures trees and their applications
- Design appropriate data structures for solving computing problems
- Analyze the operations of Linear Data structures: Stack, Queue and Linked List and their applications

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Data structures, Algorithms, and applications in C++, Sartaj Sahni, Universities Press, 2nd Edition, 2005.

Reference Books:

1. **Data structures, Algorithms, and applications in C++,** Sartaj Sahni, Mc. Graw Hill, 2000.
2. **Object Oriented Programming with C++,** E.Balaguruswamy**,** TMH, 6th Edition, 2013.
3. **Programming in C++,** E.Balaguruswamy. TMH, 4th, 2010.

DSP ALGORITHMS and ARCHITECTURE
VII Semester (EC)

[As per Choice Based Credit System (CBCS) scheme]

Course Code	18EC735	CIE Marks	40
Number of Lecture Hours/Week	03	Exam Marks	60
Total Number of Lecture Hours	40 (08 Hours per Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course will enable students to:

- Figure out the knowledge and concepts of digital signal processing techniques.
- Understand the computational building blocks of DSP processors and its speed issues.
- Understand the various addressing modes, peripherals, interrupts and pipelining structure of TMS320C54xx processor.
- Learn how to interface the external devices to TMS320C54xx processor in various modes.
- Understand basic DSP algorithms with their implementation.

Module -1	RBT Level
Introduction to Digital Signal Processing: Introduction, A Digital Signal – Processing System, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation. **Computational Accuracy in DSP Implementations:** Number Formats for Signals and Coefficients in DSP Systems, Dynamic Range and Precision, Sources of Error in DSP Implementation.	L1, L2
Module -2	
Architectures for Programmable Digital Signal – Processing Devices: Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External Interfacing.	L1, L2
Module -3	
Programmable Digital Signal Processors: Introduction, Commercial Digital Signal-processing Devices, Data Addressing Modes of TMS32OC54XX, Memory Space of TMS32OC54xx Processors, Program Control. Detail Study of TMS320C54X & 54xx Instructions and Programming, On – Chip Peripherals, Interrupts of TMS32OC54XX Processors, Pipeline Operation of TMS32OC54xx Processor.	L1, L2
Module -4	

Implementation of Basic DSP Algorithms: Introduction, The Q – notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case). **Implementation of FFT Algorithms:** Introduction, An FFT Algorithm for DFT Computation, Overflow and Scaling, Bit – Reversed Index. Generation & Implementation on the TMS32OC54xx.	**L1, L2**
Module -5	
Interfacing Memory and Parallel I/O Peripherals to Programmable DSP Devices: Introduction, Memory Space Organization, External Bus Interfacing Signals. Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I/O Direct Memory Access (DMA). **Interfacing and Applications of DSP Processors:** Introduction, Synchronous Serial Interface, A CODEC Interface Circuit, DSP Based Bio-telemetry Receiver, A Speech Processing System, An Image Processing System.	**L1, L2**

Course Outcomes: At the end of this course, students would be able to

- Comprehend the knowledge and concepts of digital signal processing techniques.
- Apply the knowledge of DSP computational building blocks to achieve speed in DSP architecture or processor.
- Apply knowledge of various types of addressing modes, interrupts, peripherals and pipelining structure of TMS320C54xx processor.
- Develop basic DSP algorithms using DSP processors.
- Discuss about synchronous serial interface and multichannel buffered serial port (McBSP) of DSP device.
- Demonstrate the programming of CODEC interfacing.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

"Digital Signal Processing", Avatar Singh and S. Srinivasan, Thomson Learning, 2004.

Reference Books:

1. "Digital Signal Processing: A practical approach", Ifeachor E. C., Jervis B. W Pearson-Education, PHI, 2002.
2. "Digital Signal Processors", B Venkataramani and M Bhaskar, TMH, 2nd, 2010
3. "Architectures for Digital Signal Processing", Peter Pirsch John Wiley, 2008

Professional Electives – 3

IoT & WIRELESS SENSOR NETWORKS
B.E., VII Semester (EC/TC)

[As per Choice Based Credit System (CBCS) Scheme]

Course Code	18EC741	CIE Marks	40
Number of Lecture Hours/Week	03	SEE Marks	60
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course will enable students to:
- Describe the OSI Model for IoT/M2M Systems.
- Understand the architecture and design principles for device supporting IoT.
- Develop competence in programming for IoT Applications.
- Identify the uplink and downlink communication protocols which best suits the specific application of IOT / WSNs.

Module-1	RBT Levels
Overview of Internet of Things: IoT Conceptual Framework, IoT Architectural View, Technology Behind IoT, Sources of IoT,M2M communication, Examples of IoT. Modified OSI Model for the IoT/M2M Systems, data enrichment, data consolidation and device management at IoT/M2M Gateway, web communication protocols used by connected IoT/M2M devices, Message communication protocols (CoAP-SMS, CoAP-MQ, MQTT, XMPP) for IoT/M2M devices. – Refer Chapter 1, 2 and 3 of Text 1.	**L1, L2**
Module-2	
Architecture and Design Principles for IoT: Internet connectivity, Internet-based communication,IPv4, IPv6,6LoWPAN protocol, IP Addressing in the IoT, Application layer protocols: HTTP, HTTPS,FTP,TELNET and ports. **Data Collection, Storage and Computing using a Cloud Platform:** Introduction, Cloud computing paradigm for data collection, storage and computing, Cloud service models, IoT Cloud- based data collection, storage and computing services using Nimbits. - Refer Chapter 4 and 6 of Text 1.	**L1, L2**
Module-3	
Prototyping and Designing Software for IoT Applications: Introduction, Prototyping Embedded device software, Programming Embedded Device Arduino Platform using IDE, Reading data from sensors and devices, Devices, Gateways, Internet and Web/Cloud services software development. Programming MQTT clients and MQTT server. Introduction to IoT privacy and security. Vulnerabilities, security requirements and threat analysis, IoT Security Tomography and layered attacker model. - Refer Chapter 9 and 10 of Text 1.	**L1, L2, L3**

Module-4	
Overview of Wireless Sensor Networks: Challenges for Wireless Sensor Networks, Enabling Technologies for Wireless Sensor Networks. **Architectures**: Single-Node Architecture - Hardware Components, Energy Consumption of Sensor Nodes, Operating Systems and Execution Environments, Network Architecture-Sensor Network Scenarios, Optimization Goals and Figures of Merit, Design principles for WSNs, Service interfaces of WSNs Gateway Concepts. - Refer Chapter 1, 2, 3 of Text 2.	**L1, L2, L3**
Module-5	
Communication Protocols: Physical Layer and Transceiver Design Considerations, MAC Protocols for Wireless Sensor Networks, Low Duty Cycle Protocols And Wakeup Concepts - S-MAC , The Mediation Device Protocol, Wakeup Radio Concepts, Contention based protocols(CSMA,PAMAS), Schedule based protocols (LEACH, SMACS, TRAMA) Address and Name Management in WSNs, Assignment of MAC Addresses, Routing Protocols- Energy-Efficient Routing, Geographic Routing, Hierarchical networks by clustering. - Refer Chapter 4, 5, 7 and 11 of Text 2.	**L1, L2, L3**

Course Outcomes: At the end of the course, students will be able to:

- Understand choice and application of IoT & M2M communication protocols.
- Describe Cloud computing and design principles of IoT.
- Awareness of MQTT clients, MQTT server and its programming.
- Develop an architecture and its communication protocols of of WSNs.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Raj Kamal, ”Internet of Things-Architecture and design principles”, McGraw Hill Education.
2. Holger Karl & Andreas Willig, "Protocols And Architectures for Wireless Sensor Networks", John Wiley, 2005.

Reference Books:

1. Feng Zhao & Leonidas J. Guibas, “Wireless Sensor Networks- An Information Processing Approach", Elsevier, 2007.
2. Kazem Sohraby, Daniel Minoli, & Taieb Znati, “Wireless Sensor Networks-Technology, Protocols, And Applications”, John Wiley, 2007.
3. Anna Hac, “Wireless Sensor Network Designs”, John Wiley, 2003.

AUTOMOTIVE ELECTRONICS
B.E., VII Semester (EC/TC)

[Choice Based Credit System (CBCS) scheme]

Course Code	**18EC742**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**3**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (8 Hours /Module)**	**Exam Hours**	**03**
CREDITS – 03			

Course objectives: This course will enable students to:

- Understand the basics of automobile dynamics and design electronics to complement those features.
- Design and implement the electronics that attribute the reliability, safety, and smartness to the automobiles, providing add-on comforts.

Module -1	**RBT Level**
Automotive Fundamentals Overview – Evolution of Automotive Electronics, Automobile Physical Configuration, Survey of Major Automotive Systems, The Engine – Engine Block, Cylinder Head, Four Stroke Cycle, Engine Control, Ignition System - Spark plug, High voltage circuit and distribution, Spark pulse generation, Ignition Timing, Diesel Engine, Drive Train - Transmission, Drive Shaft, Differential, Suspension, Brakes, Steering System (Text 1: Chapter1), Starter Battery –Operating principle: **(Text 2: Pg. 407-410)** **The Basics of Electronic Engine Control –** Motivation for Electronic Engine Control – Exhaust Emissions, Fuel Economy, Concept of an Electronic Engine control system, Definition of General terms, Definition of Engine performance terms, Engine mapping, Effect of Air/Fuel ratio, spark timing and EGR on performance, Control Strategy, Electronic Fuel control system, Analysis of intake manifold pressure, Electronic Ignition. **(Text 1: Chapter 5)**	**L1, L2**
Module -2	
Automotive Sensors – Automotive Control System applications of Sensors and Actuators – Variables to be measured, Airflow rate sensor, Strain Gauge MAP sensor, Engine Crankshaft Angular Position Sensor, Magnetic Reluctance Position Sensor, Hall effect Position Sensor, Shielded Field Sensor, Optical Crankshaft Position Sensor, Throttle Angle Sensor (TAS), Engine Coolant Temperature (ECT) Sensor, Exhaust Gas Oxygen (O2/EGO) Lambda Sensors, Piezoelectric Knock Sensor. **(Text 1: Chapter 6)** **Automotive Engine Control Actuators –** Solenoid, Fuel Injector, EGR Actuator, Ignition System **(Text 1: Chapter 6)**	**L1, L2**
Module -3	
Digital Engine Control Systems – Digital Engine control features, Control modes for fuel Control (Seven Modes), EGR Control, Electronic	**L1, L2**

Ignition Control - Closed loop Ignition timing, Spark Advance Correction Scheme, Integrated Engine Control System - Secondary Air Management, Evaporative Emissions Canister Purge, Automatic System Adjustment, System Diagnostics. **(Text 1: Chapter 7)** **Control Units –** Operating conditions, Design, Data processing, Programming, Digital modules in the Control unit, Control unit software. **(Text 2: Pg. 196-207)**	
Module -4	
Automotive Networking –Bus Systems – Classification, Applications in the vehicle, Coupling of networks, Examples of networked vehicles **(Text 2: Pg. 85-91),** Buses - CAN Bus, LIN Bus, MOST Bus, Bluetooth, Flex Ray, Diagnostic Interfaces. **(Text 2: Pg. 92-151)** **Vehicle Motion Control** – Typical Cruise Control System, Digital Cruise Control System, Digital Speed Sensor, Throttle Actuator, Digital Cruise Control configuration, Cruise Control Electronics (Digital only), Antilock Brake System (ABS) **(Text 1: Chapter 8)**	**L1,L2**
Module -5	
Automotive Diagnostics–Timing Light, Engine Analyzer, On-board diagnostics, Off-board diagnostics, Expert Systems, Occupant Protection Systems – Accelerometer based Air Bag systems. **(Text 1: Chapter 10)** **Future Automotive Electronic Systems** – Alternative Fuel Engines, Electric and Hybrid vehicles, Fuel cell powered cars, Collision Avoidance Radar warning Systems, Low tire pressure warning system, Heads Up display, Speech Synthesis, Navigation – Navigation Sensors - Radio Navigation, Signpost navigation, dead reckoning navigation, Voice Recognition Cell Phone dialing, Advanced Cruise Control, Stability Augmentation, Automatic driving Control **(Text 1: Chapter 11)**	**L1, L2,L3**

Course Outcomes: At the end of the course, students will be able to:

- Acquire an overview of automotive components, subsystems, and basics of Electronic Engine Control in today's automotive industry.
- Use available automotive sensors and actuators while interfacing with microcontrollers / microprocessors during automotive system design.
- Understand the networking of various modules in automotive systems, communication protocols and diagnostics of the sub systems.
- Design and implement the electronics that attribute the reliability, safety, and smartness to the automobiles, providing add-on comforts and get fair idea on future Automotive Electronic Systems.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. William B. Ribbens, “Understanding Automotive Electronics”, 6th Edition, Elsevier Publishing.
2. Robert Bosch Gmbh (Ed.) Bosch Automotive Electrics and Automotive Electronics Systems and Components, Networking and Hybrid Drive, 5th edition, John Wiley & Sons Inc., 2007.

MULTIMEDIA COMMUNICATION
VII Semester (EC/TC)

[As per Choice Based Credit System (CBCS) scheme]

Course Code	18EC743	CIE Marks	40
Number of Lecture Hours/Week	03	Exam Marks	60
Total Number of Lecture Hours	40 (08 Hours per Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course will enable students to:

- Understand the importance of multimedia in today's online and offline information sources and repositories.
- Understand the how Text, Audio, Image and Video information can be represented digitally in a computer so that it can be processed, transmitted and stored efficiently.
- Understand the Multimedia Transport in Wireless Networks
- Understand the Real-time multimedia network applications.
- Understand the Different network layer based application.

Module -1	RBT Level
Multimedia Communications: Introduction, Multimedia information representation, multimedia networks, multimedia applications, Application and networking terminology. (**Chapter 1 of Text 1)**	**L1,L2**
Module -2	
Information Representation: Introduction, Digitization principles, Text, Images, Audio and Video. **(Chapter 2 of Text 1)**	**L1,L2**
Module -3	
Text and Image Compression: Introduction, Compression principles, text compression, image Compression. **(Chapter 3 of Text 1)** **Distributed Multimedia Systems:** Introduction, main Features of a DMS, Resource management of DMS, Networking, Multimedia Operating Systems. **(Chapter 4 - Sections 4.1 to 4.5 of Text 2)**	**L1,L2**
Module -4	
Audio and video compression: Introduction, Audio compression, video compression, video compression principles, video compression.**(Chapter 4 of Text 1)**	**L1,L2**
Module -5	

Multimedia Information Networks: Introduction, LANs, Ethernet, Token ring, Bridges, FDDI High-speed LANs, LAN protocol **(Chap. 8 of Text 1).** **The Internet:** Introduction, IP Datagrams, Fragmentation, IP Address, ARP and RARP, QoS Support, IPv8. **(Chap. 9 of Text 1)**	**L1,L2**

Course Outcomes: After studying this course, students will be able to:

- Understand basics of different multimedia networks and applications.
- Understand different compression techniques to compress audio and video.
- Describe multimedia Communication across Networks.
- Analyse different media types to represent them in digital form.
- Compress different types of text and images using different compression techniques.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. Multimedia Communications- Fred Halsall, Pearson Education, 2001, ISBN - 9788131709948.
2. Multimedia Communication Systems- K. R. Rao, Zoran S. Bojkovic, Dragorad A. Milovanovic, Pearson Education, 2004. ISBN -9788120321458.

Reference Book:

Multimedia: Computing, Communications and Applications- Raifsteinmetz, Klara Nahrstedt, Pearson Education, 2002. ISBN -978817758

CRYPTOGRAPHY
VII Semester (EC/TC)

[As per Choice Based Credit System (CBCS) scheme]

Course Code	**18EC744**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**Exam Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Objectives: This course will enable students to:

- Understand the basics of symmetric key and public key cryptography.
- Explain classical cryptography algorithms.
- Acquire knowledge of mathematical concepts required for cryptography.
- Describe pseudo random sequence generation technique.
- Explain symmetric and asymmetric cryptography algorithms.

Module -1	**RBT Level**
Classical Encryption Techniques: Symmetric cipher model, Substitution techniques, Transposition techniques **(Text 1: Chapter 1)** **Basic Concepts of Number Theory and Finite Fields:** Euclidean algorithm, Modular arithmetic **(Text 1: Chapter 3)**	**L1,L2**
Module -2	
SYMMETRIC CIPHERS: Traditional Block Cipher structure, Data encryption standard (DES), The AES Cipher. **(Text 1: Chapter 2: Section1, 2, Chapter 4: Section 2, 3, 4)**	**L1,L2**
Module -3	
Basic Concepts of Number Theory and Finite Fields: Groups, Rings and Fields, Finite fields of the form GF(p), Prime Numbers, Fermat's and Euler's theorem, discrete logarithm. **(Text 1: Chapter 3 and Chapter 7: Section 1, 2, 5)**	**L1,L2**
Module -4	
ASYMMETRIC CIPHERS: Principles of Public-Key Cryptosystems, The RSA algorithm, Diffie - Hellman Key Exchange, Elliptic Curve Arithmetic, Elliptic Curve Cryptography **(Text 1: Chapter 8, Chapter 9: Section 1, 3, 4)**	**L1,L2,L3**
Module -5	
Pseudo-Random-Sequence Generators and Stream Ciphers: Linear Congruential Generators, Linear Feedback Shift Registers, Design and analysis of stream ciphers, Stream ciphers using LFSRs, A5, Hughes XPD/KPD, Nanoteq, Rambutan, Additive generators, Gifford, Algorithm M, PKZIP **(Text 2: Chapter 16**)	**L1,L2, L3**

Course Outcomes: After studying this course, students will be able to:

- Explain basic cryptographic algorithms to encrypt and decrypt the data.
- Use symmetric and asymmetric cryptography algorithms to encrypt and decrypt the information.
- Apply concepts of modern algebra in cryptography algorithms.
- Apply pseudo random sequence in stream cipher algorithms.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. William Stallings , "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3
2. Bruce Schneier, "Applied Cryptography Protocols, Algorithms, and Source code in C", Wiley Publications, 2nd Edition, ISBN: 9971-51-348-X.

Reference Books:

1. Cryptography and Network Security, Behrouz A. Forouzan, TMH, 2007.
2. Cryptography and Network Security, Atul Kahate, TMH, 2003.

MACHINE LEARNING
VII Semester (EC/TC)

[As per Choice Based Credit System (CBCS) scheme]

Course Code	18EC745	CIE Marks	40
Number of Lecture Hours/Week	03	Exam Marks	60
Total Number of Lecture Hours	40 (08 Hours per Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course will enable students to:

- Acquire some concepts and techniques that are core to Machine Learning.
- Understand learning and decision trees.
- Acquire knowledge of neural networks, Bayesian techniques and instant based learning.
- Understand analytical learning and reinforced learning.

Module -1	RBT Level
Learning: Designing Learning systems, Perspectives and Issues, Concept Learning, Version Spaces and Candidate Elimination Algorithm, Inductive bias.	L1,L2
Module -2	
Decision Tree and ANN: Decision Tree Representation, Hypothesis Space Search, Inductive bias in decision tree, issues in Decision tree. Neural Network Representation, Perceptrons, Multilayer Networks and Back Propagation Algorithms.	L1,L2
Module -3	
Bayesian and Computational Learning: Bayes Theorem, Bayes Theorem Concept Learning, Maximum Likelihood, Minimum Description Length Principle, Bayes Optimal Classifier, Gibbs Algorithm, Naïve Bayes Classifier.	L1,L2
Module -4	
Instant Based Learning and Learning set of rules: K- Nearest Neighbour Learning, Locally Weighted Regression, Radial Basis Functions, Case-Based Reasoning. Sequential Covering Algorithms, Learning Rule Sets, Learning First Order Rules, Learning Sets of First Order Rules.	L1,L2
Module -5	
Analytical Learning and Reinforced Learning: Perfect Domain Theories, Explanation Based Learning, Inductive-Analytical Approaches, FOCL Algorithm, Reinforcement Learning.	L1,L2

Course outcomes: At the end of the course, students should be able to:

- Understand the core concepts of Machine learning.
- Appreciate the underlying mathematical relationships within and across Machine Learning algorithms.
- Explain paradigms of supervised and un-supervised learning.
- Recognize a real world problem and apply the learned techniques of Machine Learning to solve the problem.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Machine Learning-Tom M. Mitchell, McGraw-Hill Education, (Indian Edition), 2013.

Reference Books:

1. **Introduction to Machine Learning-** Ethem Alpaydin, 2nd Ed., PHI Learning Pvt. Ltd., 2013.
2. **The Elements of Statistical Learning-**T. Hastie, R. Tibshirani, J. H. Friedman, Springer; 1st edition, 2001.

COMPUTER NETWORKS LAB

SEMESTER – VII (EC)
[As per Choice Based Credit System (CBCS) Scheme]

Course Code	18ECL76	CIE Marks	40
Number of Lecture Hours/Week	02 Hr Tutorial (Instructions) + 02 Hours Laboratory	SEE Marks	60
RBT Levels	L1, L2, L3	Exam Hours	03

CREDITS – 02

Course objectives: This course will enable students to:

- Choose suitable tools to model a network and understand the protocols at various OSI reference levels.
- Design a suitable network and simulate using a Network simulator tool.
- Simulate the networking concepts and protocols using C/C++ programming.
- Model the networks for different configurations and analyze the results.

Laboratory Experiments

PART-A: Simulation experiments using NS2/ NS3/ OPNET/ NCTUNS/ NetSim/QualNet or any other equivalent tool

1. Implement a point to point network with four nodes and duplex links between them. Analyze the network performance by setting the queue size and varying the bandwidth.
2. Implement a four node point to point network with links n0-n2, n1-n2 and n2-n3. Apply TCP agent between n0-n3 and UDP between n1-n3. Apply relevant applications over TCP and UDP agents changing the parameter and determine the number of packets sent by TCP/UDP.
3. Implement Ethernet LAN using n (6-10) nodes. Compare the throughput by changing the error rate and data rate.
4. Implement Ethernet LAN using n nodes and assign multiple traffic to the nodes and obtain congestion window for different sources/ destinations.
5. Implement ESS with transmission nodes in Wireless LAN and obtain the performance parameters.

PART-B: Implement the following in C/C++

1. Write a program for a HLDC frame to perform the following.

i) Bit stuffing

ii) Character stuffing.

2. Write a program for distance vector algorithm to find suitable path for

3. Implement Dijkstra's algorithm to compute the shortest routing path.
4. For the given data, use CRC-CCITT polynomial to obtain CRC code. Verify the program for the cases
   a. Without error
   b. With error
5. Implementation of Stop and Wait Protocol and Sliding Window Protocol
6. Write a program for congestion control using leaky bucket algorithm.

Course outcomes: On the completion of this laboratory course, the students will be able to:

- Use the network simulator for learning and practice of networking algorithms.
- Illustrate the operations of network protocols and algorithms using C programming.
- Simulate the network with different configurations to measure the performance parameters.
- Implement the data link and routing protocols using C programming.

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- For examination one question from software and one question from hardware or only one hardware experiments based on the complexity to be set.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

VLSI LAB

B.E., VII Semester EC

[As per Choice Based Credit System (CBCS) Scheme]

Course Code	**18ECL77**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**02 Hr Tutorial (Instructions) + 02 Hours Laboratory**	**SEE Marks**	**60**
RBT Levels	**L1, L2, L3**	**Exam Hours**	**03**

CREDITS – 02

Course objectives: This course will enable students to:

- Design, model, simulate and verify CMOS digital circuits
- Design layouts and perform physical verification of CMOS digital circuits
- Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level net list
- Perform RTL-GDSII flow and understand the stages in ASIC design

Experiments can be conducted using any of the following or equivalent design tools: Cadence/Synopsis/Mentor Graphics/Microwind

Laboratory Experiments

Part – A

Analog Design

Use any VLSI design tools to carry out the experiments, use library files and technology files below 180 nm.

1. a) Capture the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of inverter with Wn = Wp, Wn = 2Wp, Wn = Wp/2 and length at selected technology. Carry out the following:

   a. Set the input signal to a pulse with rise time, fall time of 1ns and pulse width of 10ns and time period of 20ns and plot the input voltage and output voltage of designed inverter?

   b. From the simulation results compute tpHL, tpLH and td for all three geometrical settings of width?

   c. Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter?

1. b) Draw layout of inverter with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

2. a) Capture the schematic of 2-input CMOS NAND gate having similar delay as that of CMOS inverter computed in experiment 1. Verify the functionality of NAND gate and also find out the delay td for all four possible combinations of input vectors. Table the results. Increase the drive strength to 2X and 4X and tabulate the results.

2. b) Draw layout of NAND with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

3. a) Capture schematic of Common Source Amplifier with PMOS Current Mirror Load and find its transient response and AC response? Measures the Unity Gain Bandwidth (UGB), amplification factor by varying transistor geometries, study the impact of variation in width to UGB.

3. b) Draw layout of common source amplifier, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

4. a) Capture schematic of two-stage operational amplifier and measure the following:

a. UGB
b. dB bandwidth
c. Gain margin and phase margin with and without coupling capacitance
d. Use the op-amp in the inverting and non-inverting configuration and verify its functionality
e. Study the UGB, 3dB bandwidth, gain and power requirement in op-amp by varying the stage wise transistor geometries and record the observations.

4. b) Draw layout of two-stage operational amplifier with minimum transistor width set to 300 (in 180/90/45 nm technology), choose appropriate transistor geometries as per the results obtained in 4.a. Use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

Part - B

Digital Design

Carry out the experiments using semicustom design flow or ASIC design flow, use technology library 180/90/45nm and below

Note: The experiments can also be carried out using FPGA design flow, it is required to set appropriate constraints in FPGA advanced synthesis options

1. Write verilog code for 4-bit up/down asynchronous reset counter and carry out the following:

a. Verify the functionality using test bench
b. Synthesize the design by setting area and timing constraint. Obtain the gate level netlist, find the critical path and maximum frequency of operation. Record the area requirement in terms of number of cells required and properties of each cell in terms of driving strength, power and area requirement.
c. Perform the above for 32-bit up/down counter and identify the critical path,

delay of critical path, and maximum frequency of operation, total number of cells required and total area.

2. Write verilog code for 4-bit adder and verify its functionality using test bench. Synthesize the design by setting proper constraints and obtain the net list. From the report generated identify critical path, maximum delay, total number of cells, power requirement and total area required. Change the constraints and obtain optimum synthesis results.

3. Write verilog code for UART and carry out the following:

a. Perform functional verification using test bench
b. Synthesize the design targeting suitable library and by setting area and timing constraints
c. For various constrains set, tabulate the area, power and delay for the synthesized netlist
d. Identify the critical path and set the constraints to obtain optimum gate level netlist with suitable constraints

4. Write verilog code for 32-bit ALU supporting four logical and four arithmetic operations,
use case statement and if statement for ALU behavioral modeling.

a. Perform functional verification using test bench
b. Synthesize the design targeting suitable library by setting area and timing constraints
c. For various constrains set, tabulate the area, power and delay for the synthesized netlist
d. Identify the critical path and set the constraints to obtain optimum gate level netlist with suitable constraints

Compare the synthesis results of ALU modeled using IF and CASE statements.

5. Write verilog code for Latch and Flip-flop, Synthesize the design and compare the synthesis report (D, SR, JK).

6. For the synthesized netlist carry out the following for any two above experiments:
a. Floor planning (automatic), identify the placement of pads
b. Placement and Routing, record the parameters such as no. of layers used for routing, flip method for placement of standard cells, placement of standard cells, routes of power and ground, and routing of standard cells
c. Physical verification and record the LVS and DRC reports
d. Perform Back annotation and verify the functionality of the design
e. Generate GDSII and record the number of masks and its color composition

Course outcomes: On the completion of this laboratory course, the students will be able to:

- Design and simulate combinational and sequential digital circuits using Verilog HDL
- Understand the Synthesis process of digital circuits using EDA tool.
- Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level net list
- Design and simulate basic CMOS circuits like inverter, common source amplifier and differential amplifiers.
- Perform RTL-GDSII flow and understand the stages in ASIC design.

OPEN ELECTIVE-B OFFERED BY EC/TC BOARD

COMMUNICATION THEORY

SEMESTER – Open Elective-B

[As per Choice Based Credit System (CBCS) scheme]

Course Code	18EC751	CIE Marks	40
Number of Lecture Hours/Week	3	SEE Marks	60
Total Number of Lecture Hours	40 (8 Hours/Module)	Exam Hours	03

CREDITS – 03

Course objectives: This course will enable students to:

- Describe essential elements of an electronic communications.
- Understand Amplitude, Frequency & Phase modulations, and Amplitude demodulation.
- Explain the basics of sampling and quantization.
- Understand the various digital modulation schemes.
- The concepts of wireless communication.

Module -1	RBT Level
Introduction to Electronic Communications: Historical perspective, Electromagnetic frequency spectrum, signal and its representation, Elements of electronic communications system, primary communication resources, signal transmission concepts, Analog and digital transmission, Modulation, Concept of frequency translation, Signal radiation and propagation **(Text 1: 1.1 to1.10)**	**L1, L2**
Module -2	
Noise: Classification and source of noise **(TEXT1:3.1)** **Amplitude Modulation Techniques:** Types of analog modulation, Principle of amplitude modulation, AM power distribution, Limitations of AM, **(TEXT 1: 4.1, 4.2, 4.4, 4.6)** **Angle Modulation Techniques:** Principles of Angle modulation, Theory of FM-basic Concepts, Theory of phase modulation **(TEXT1: 5.1, 5.2, 5.5)** **Analog Transmission and Reception:** AM Radio transmitters, AM Radio Receivers **(TEXT 1: 6.1, 6.2)**	**L1, L2**
Module -3	
Sampling Theorem and pulse Modulation Techniques: Digital Versus analog Transmissions, Sampling Theorem, Classification of pulse modulation techniques, PAM, PWM, PPM, PCM, Quantization of signals **(TEXT 1: 7.1 to 7.8)**	**L1, L2**
Module -4	

Digital Modulation Techniques: Types of digital Modulation, ASK,FSK,PSK,QPSK **(TEXT 1: 9.1 to 9.5)** **Source and Channel Coding:** Objective of source coding, source coding technique, Shannon's source coding theorem, need of channel coding, Channel coding theorem, error control and coding **(TEXT 1: 11.1 to 11.3, 11.8, 11.9, 11.12)**	**L1,L2**
Module -5	
Evolution of wireless communication systems: Brief History of wireless communications, Advantages of wireless communication, disadvantages of wireless communications, wireless network generations, Comparison of wireless systems, Evolution of next-generation networks, Applications of wireless communication **(TEXT 2: 1.1 to 1.7)** **Principles of Cellular Communications:** Cellular terminology, Cell structure and Cluster, Frequency reuse concept, Cluster size and system capacity, Method of locating cochannel cells, Frequecy reuse distance **(TEXT 2: 4.1 to 4.7)**	**L1, L2**

Course Outcomes: At the end of the course, students will be able:

- Describe operation of communication systems.
- Understand the techniques of Amplitude and Angle modulation.
- Understand the concept of sampling and quantization.
- Understand the concepts of different digital modulation techniques.
- Describe the principles of wireless communications system.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. Analog and Digital Communications by T L Singal, McGraw Hill Education (India) Private Limited.
2. Wireless Communications by T L Singal, McGraw Hill Education (India) Private Limited.

Reference Books:

1. Modern Digital and Analog Communication Systems B. P. Lathi, Oxford University Press., 4th ed, 2010,
2. Communication Systems: Analog and Digital, R.P.Singh and S.Sapre: TMH 2nd edition, 2007
3. Introduction to Wireless Telecommunications systems and Networks by Gray J Mullett, Cengage learning.

NEURAL NETWORKS
VII Semester – Open Elective-B

[As per Choice Based Credit System (CBCS) scheme]

Course Code	**18EC752**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**Exam Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Objectives: This course will enable students to:

- Understand the basics of ANN and comparison with Human brain.
- Acquire knowledge on Generalization and function approximation of various ANN architectures.
- Understand reinforcement learning using neural networks
- Acquire knowledge of unsupervised learning using neural networks.

Module -1	**RBT Level**
Introduction: Biological Neuron – Artificial Neural Model -Types of activation functions – **Architecture**: Feedforward and Feedback, Convex Sets, Convex Hull and Linear Separability, Non-Linear Separable Problem. XOR Problem, Multilayer Networks. **Learning:** Learning Algorithms, Error correction and Gradient Descent Rules,	**L1,L2**
Module -2	
Supervised Learning: Perceptron learning and Non Separable sets, α-Least Mean Square Learning, MSE Error surface, Steepest Descent Search, μ-LMS approximate to gradient descent, Application of LMS to Noise Cancelling, Multi-layered Network Architecture, Backpropagation Learning Algorithm, Practical consideration of BP algorithm.	**L1,L2,L3**
Module -3	
Support Vector Machines and Radial Basis Function: Learning from Examples, Statistical Learning Theory, Support Vector Machines, SVM application to Image Classification, Radial Basis Function Regularization theory, Generalized RBF Networks, Learning in RBFNs, RBF application to face recognition.	
Module -4	
Attractor Neural Networks: Associative Learning Attractor Associative Memory, Linear Associative memory, Hopfield Network, application of Hopfield Network, Brain State in a Box neural Network, Simulated Annealing, Boltzmann Machine, Bidirectional Associative Memory.	**L1,L2,L3**
Module -5	

Self -organization Feature Map: Maximal Eigenvector Filtering, Extracting Principal Components, Generalized Learning Laws, Vector Quantization, Self -organization Feature Maps, Application of SOM, Growing Neural Gas.	**L1,L2,L3**

Course outcomes: At the end of the course, students should be able to:

- Understand the role of neural networks in engineering, artificial intelligence, and cognitive modelling.
- Understand the concepts and techniques of neural networks through the study of the most important neural network models.
- Evaluate whether neural networks are appropriate to a particular application.
- Apply neural networks to particular application, and to know what steps to take to improve performance.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Neural Networks A Classroom Approach –Satish Kumar, McGraw Hill Education (India) Pvt. Ltd, Second Edition.

Reference Books:

1. **Introduction to Artificial Neural Systems -** J.M. Zurada, Jaico Publications 1994.
2. **Artificial Neural Networks-** B. Yegnanarayana, PHI, New Delhi 1998.